CHANDIGARH ENGINERING COLLEGE - CGC LANDRAN
ELECTRONICS AND COMMUNICATION ENGINEERING DEPARTMENT

Assignment No: 2

Subject and Subject code: Digital System Design and BTEC– 302-18
Semester: 3rd
Date on which assignment given: 04.10.2024
Date of submission of assignment: 15.10.2024

Note: Each question carries 2 marks **Total marks: 10**

Course Outcome

CO 1	Apply concepts of Boolean algebra for handling logical expressions.
CO 2	Apply working and realization of combinational logical expressions.
CO 3	Realize working flip-flops and use them in designing of sequential circuits.
CO 4	Apply fundamental concepts of logic families and architectural of programmable devices.
CO 5	Use HDL programming tool for simulation of combinational and sequential circuits

Bloom's Taxonomy Levels

L1 – Remembering, L2 – Understanding, L3 – Applying, L4 – Analyzing, L5 – Evaluating, L6 - Creating

S. No.	Questions	Marks	Relevance to CO No.	Bloom's Level
1.	Design MOD-5 Asynchronous or Ripple Counter.	**2**	**CO-3**	**L1**
2.	Why do we need A/D converters? Explain the working of Dual slope A/D converter using suitable block diagram.	**2**	**CO-4**	**L2**
3.	a) Design a 3-bit Binary to Gray Code Converter using Programmable Logic Array. b) Explain the following characteristics of Digital Logic Families: Propagation Delay and Noise Margin	**2+2=4**	**CO-4**	**L3/L2**
4.	a) Explain various data types used in VHDL. b) Implement Full Adder circuit using VHDL.	**2**	**CO 5**	**L2/L5**